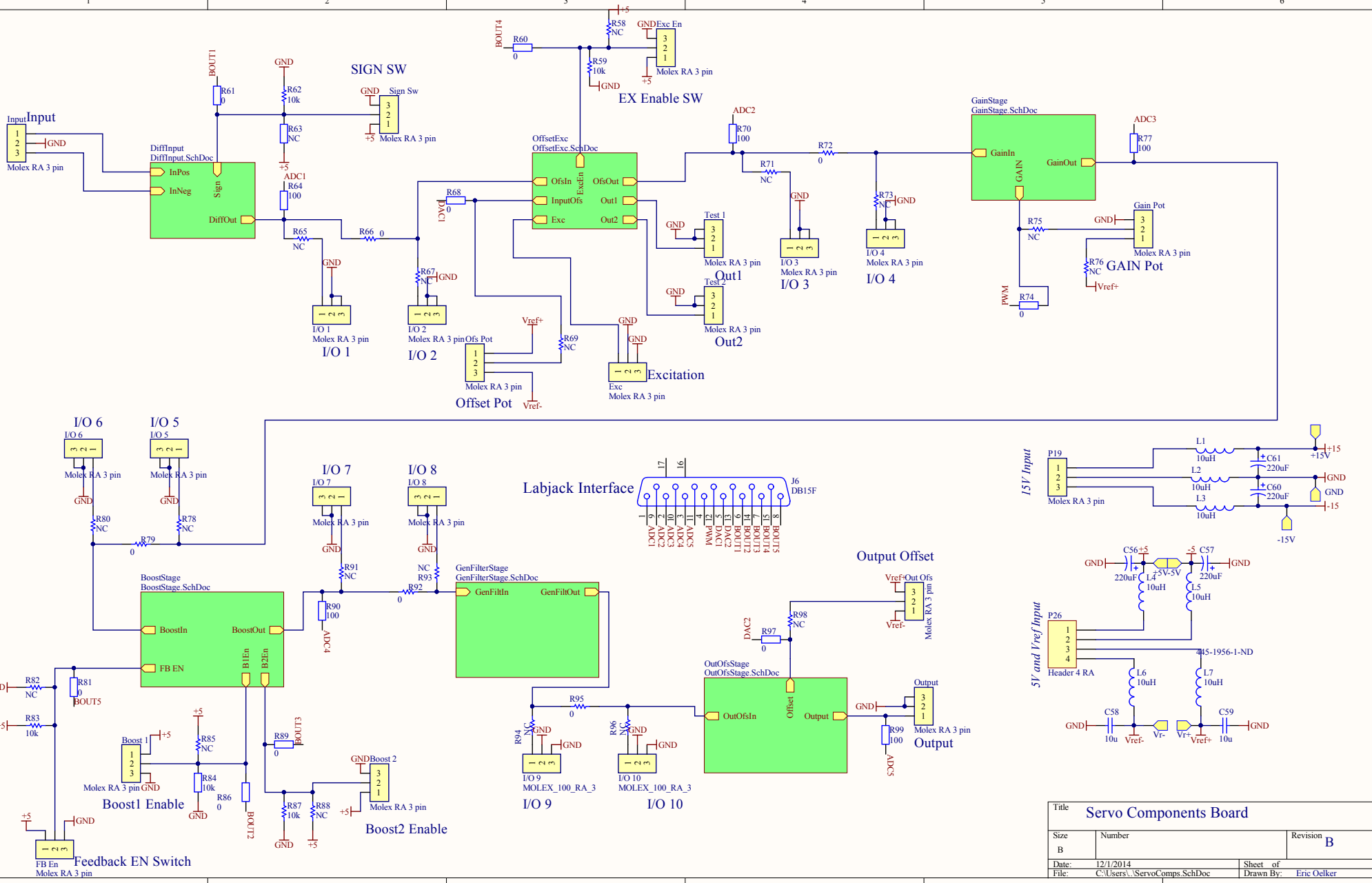
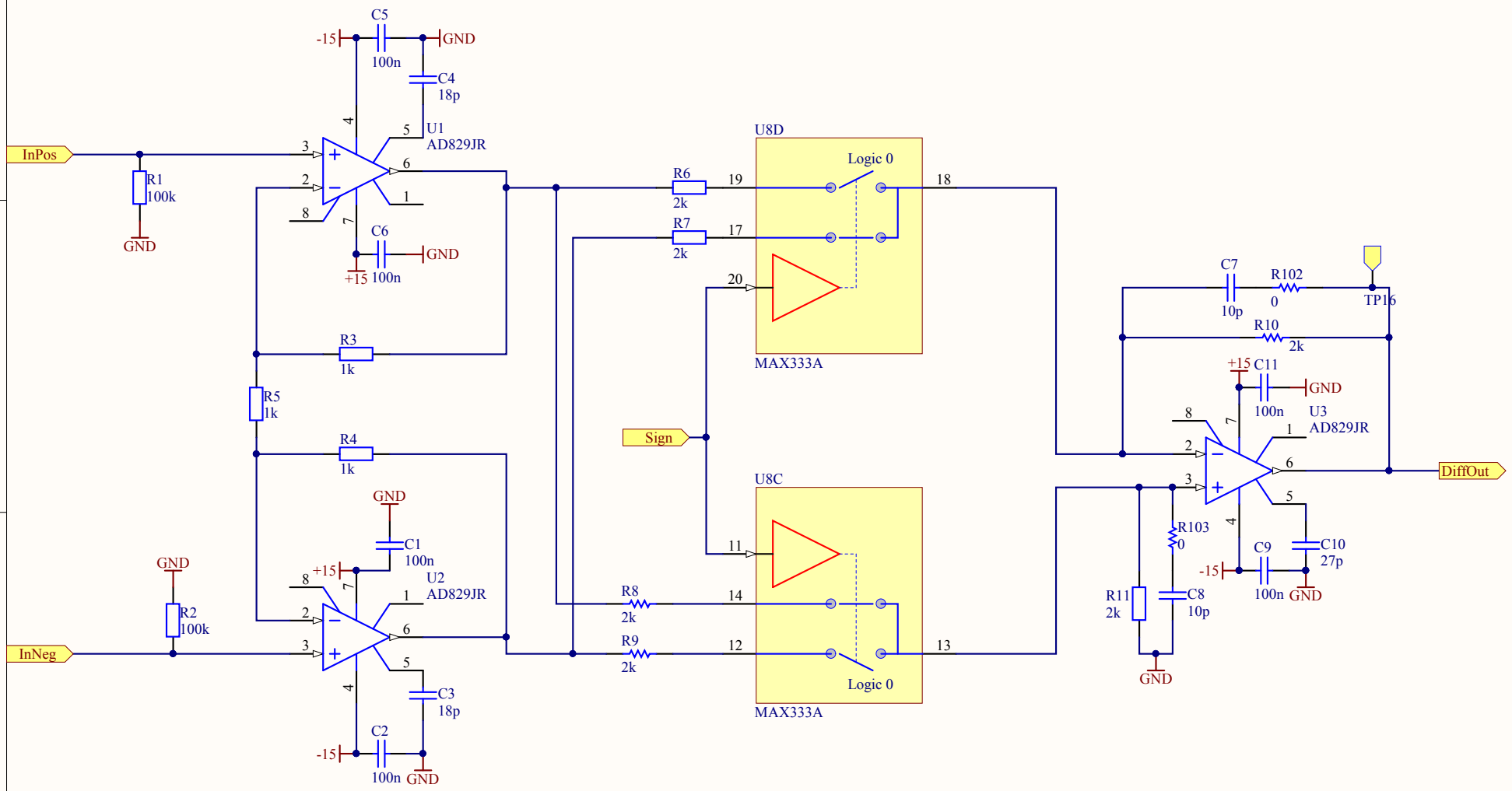
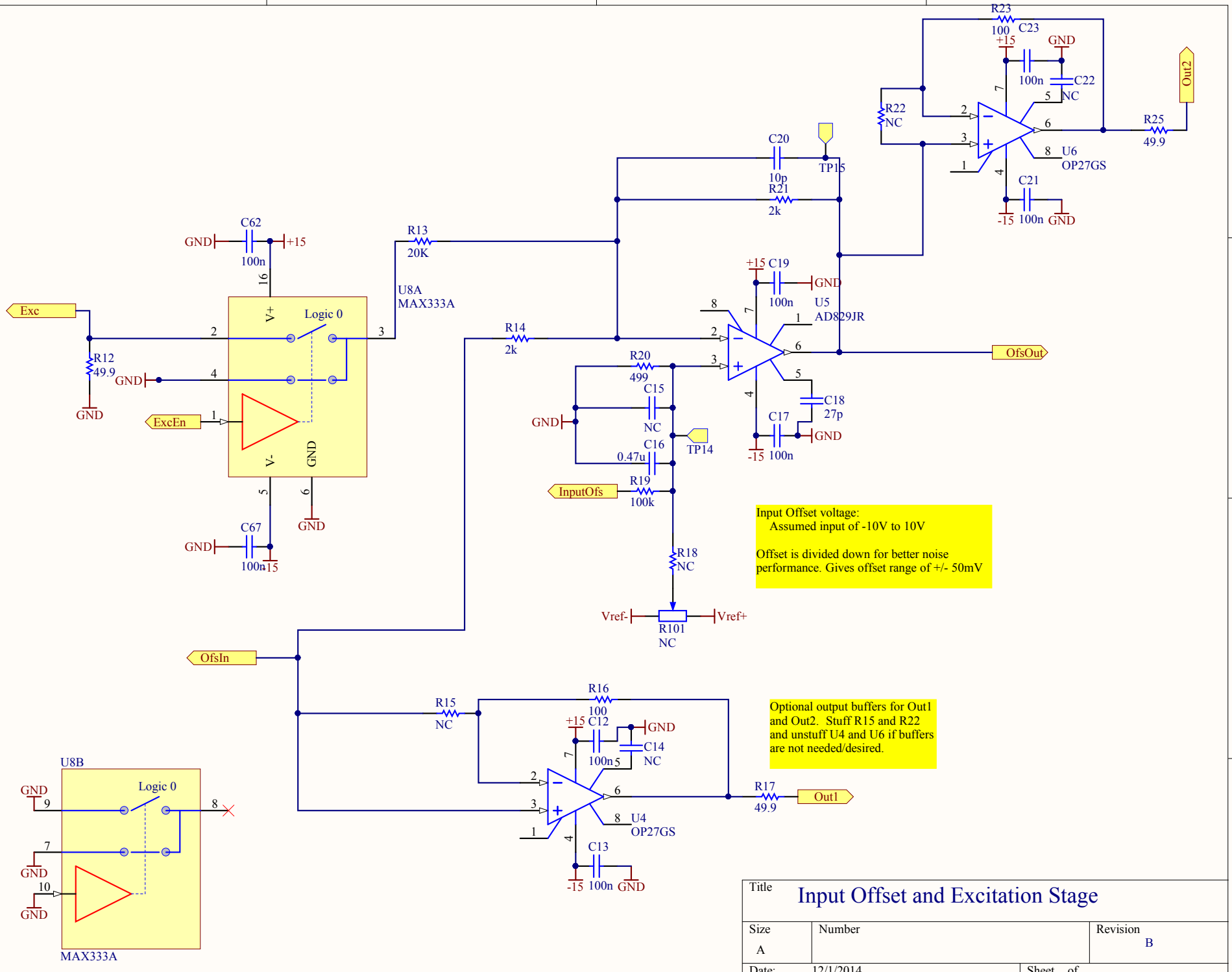

Input
DiffInput
DiffInput.SchDoc
InPos
InNeg
Sign
DiffOut
SIGN SW
Sign Sw
EX Enable SW
Exc En
OffsetExc
OffsetExc.SchDoc
OfsIn
InputOfs
Exc
OfsOut
Out1
Out2
ExcEn
GainStage
GainStage.SchDoc
GainIn
GainOut
GAIN
GAIN Pot
Test 1
Test 2
Out1
Out2
I/O 1
I/O 2
I/O 3
I/O 4
Ofs Pot
Offset Pot
Excitation
Vref+
Vref-
PWM
BOUT1
BOUT2
BOUT3
BOUT4
BOUT5
DAC1
ADC1
ADC2
ADC3
ADC4
ADC5
Molex RA 3 pin
I/O 6
I/O 5
I/O 7
I/O 8
BoostStage
BoostStage.SchDoc
BoostIn
BoostOut
FB EN
B1En
B2En
Boost 1
Boost 2
Boost1 Enable
Boost2 Enable
FB En
Feedback EN Switch
GenFilterStage
GenFilterStage.SchDoc
GenFiltIn
GenFiltOut
Labjack Interface
J6
DB15F
Output Offset
Out Ofs
OutOfsStage
OutOfsStage.SchDoc
OutOfsIn
Offset
Output
I/O 9
I/O 10
MOLEX_100_RA_3
15V Input
5V and Vref Input
P19
P26
Header 4 RA
445-1956-1-ND
+15V
-15V
+5V-5V
Title
Servo Components Board
Size
B
Number
Revision
B
Date:
12/1/2014
Sheet of
File:
C:\Users\..\ServoComps.SchDoc
Drawn By:
Eric Oelker




Stuff R5 to add up-front gain for small error signals, C3 and C4 must change accordingly. Also, R102 and R103 can be used for extra boost or whitening. C10 May need to be adjusted if gain of U3 is changed. See AD829 data sheet for details.

| | | |
|---|---|---|
| Title | Differential Input/Sign Stage | |
| Size: A | Number: | Revision: B |
| Date: 12/1/2014 | | Sheet of |
| File: C:\Users\..\DiffInput.SchDoc | | Drawn By: Eric Oelker |


R23
100
C23
+15
GND
100n
C22
NC
R22
NC
Out2
R25
49.9
U6
OP27GS
C21
-15
100n
GND
C20
10p
TP15
R21
2k
C62
GND
+15
100n
R13
20K
U8A
MAX333A
Exc
R12
49.9
GND
ExcEn
V+
Logic 0
V-
GND
C67
100n
+15
+15
C19
100n
U5
AD829JR
R14
2k
R20
499
C15
NC
C16
0.47u
TP14
C18
27p
C17
100n
-15
OfsOut
InputOfs
R19
100k
R18
NC
Vref-
Vref+
R101
NC
Input Offset voltage:
Assumed input of -10V to 10V
Offset is divided down for better noise performance. Gives offset range of +/- 50mV
OfsIn
R15
NC
R16
100
C12
100n
C14
NC
R17
49.9
Out1
U4
OP27GS
C13
-15
100n
GND
Optional output buffers for Out1 and Out2. Stuff R15 and R22 and unstuff U4 and U6 if buffers are not needed/desired.
U8B
Logic 0
MAX333A
Title
Input Offset and Excitation Stage
Size
A
Number
Revision
B
Date:
12/1/2014
Sheet of
File:
C:\Users\..\OffsetExc.SchDoc
Drawn By:
Eric Oelker

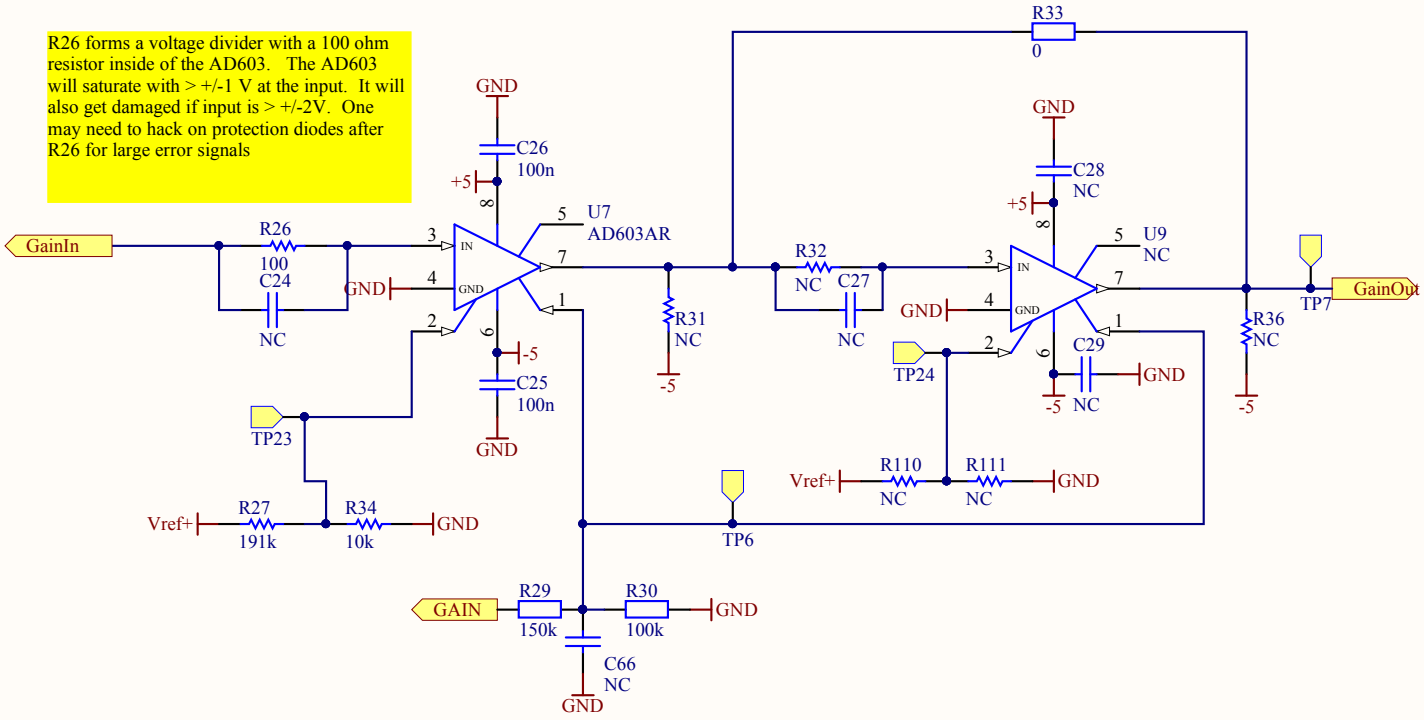
Gain control voltage:
Assumed input of 0V to 2.5V (Adjust R29 and R30 voltage divider if other range is desired)
Vg = 0 to 2.5 mV for -10 dB to 30 dB of gain.

Maximum output = +/-3V

Gain = Vg*16-10 (in dB)

Optional 2nd gain stage. See data sheet for optimal biasing at pin 2 for 2x gain stage.

R26 forms a voltage divider with a 100 ohm resistor inside of the AD603. The AD603 will saturate with > +/-1 V at the input. It will also get damaged if input is > +/-2V. One may need to hack on protection diodes after R26 for large error signals




R27 and R34 give 0.5V at GNeg input.

If GAIN = 0-2.5V, R29 and R30 give 0-1V at GPos input (This is the range on the signal from the LabJack Interface board).

This gives a control voltage from -0.5V to 0.5V.

| | | |
|---|---|---|
| Title: Variable Gain Stage | | |
| Size: A | Number: | Revision: B |
| Date: 12/1/2014 | | Sheet of |
| File: C:\Users\..\GainStage.SchDoc | | Drawn By: Eric Oelker |

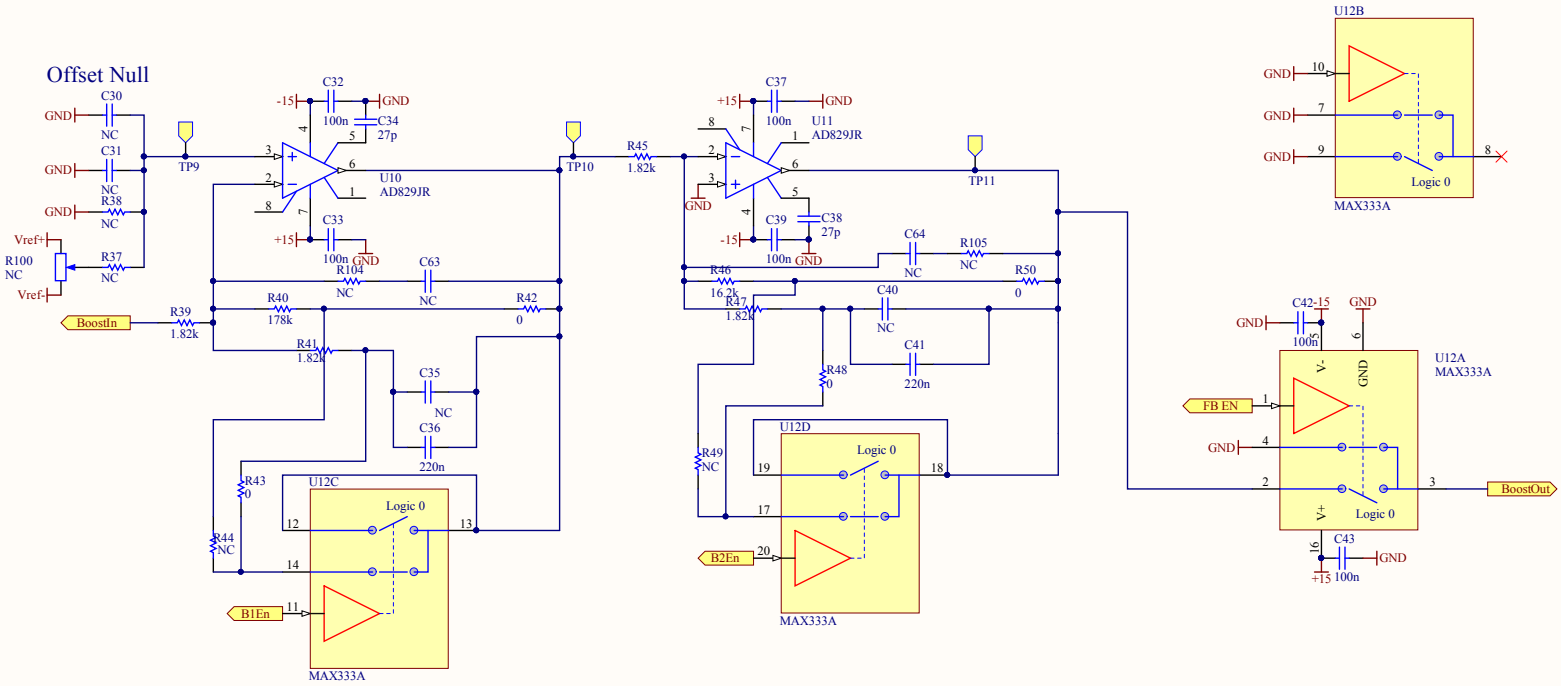
Example: Switchable Boost stage
(Eqns Assume R61=R62 And R64>>R62)
Logic = 0: unity gain follower if R64>>R63
Gain = 1

Logic = 1: boost filter
High freq gain: 1 Low freq gain = (R64)/R62
Zero = 1/(2*pi*101n*R62*(C22+C24+C39))
Pole = 1/(2*pi*101n*R64*(C22+C24+C39)).

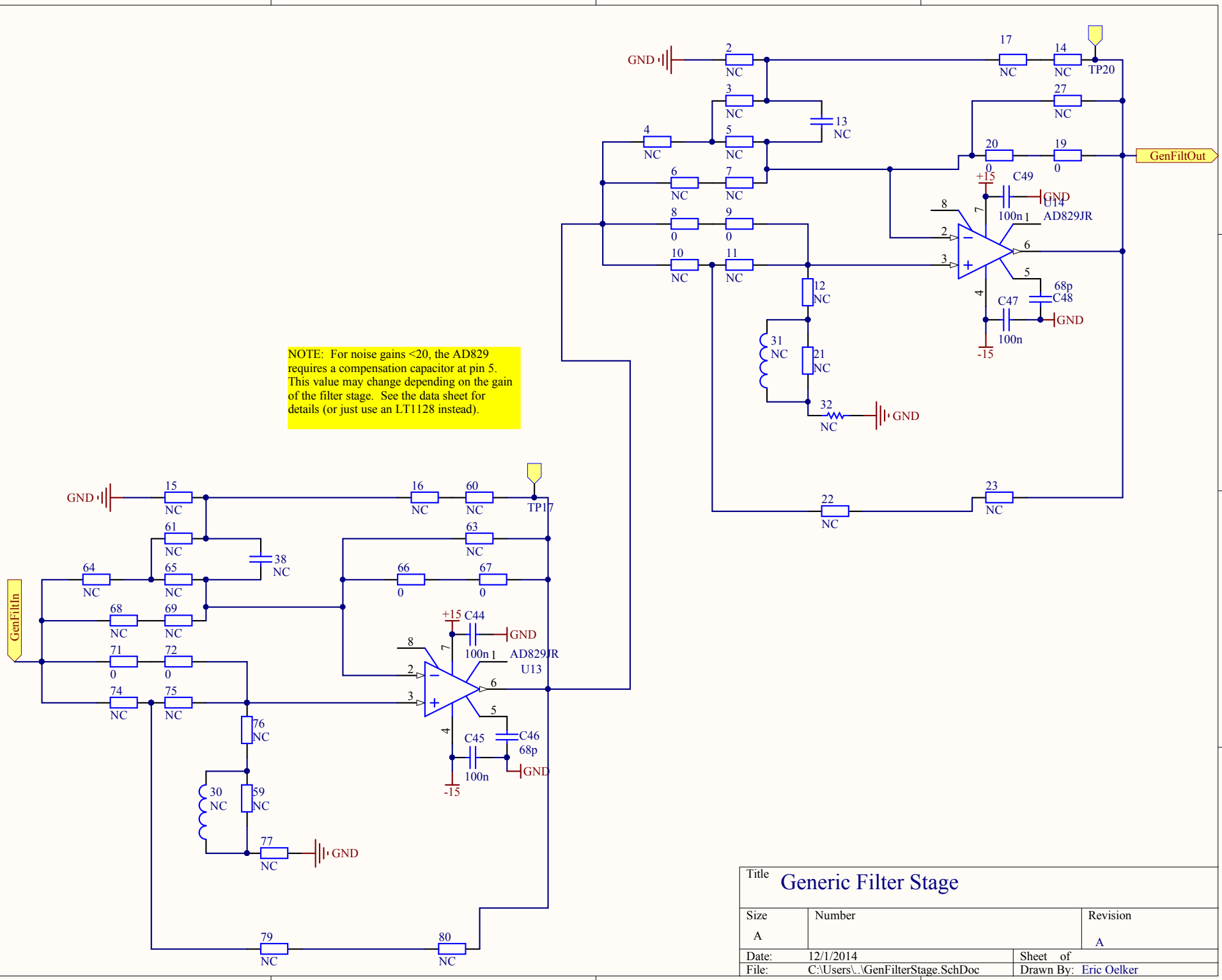
Example: Switchable Integration Stage

Logic = 0: Boost Filter (Eqns Assume R68=R67 And R69>>R67)
HF gain = 1 Low Freq Gain = R69/R67
Pole = 1/(2*pi*(C21+C25)*R69)
Zero = 1/(2*pi*(C21+C25)*R67)

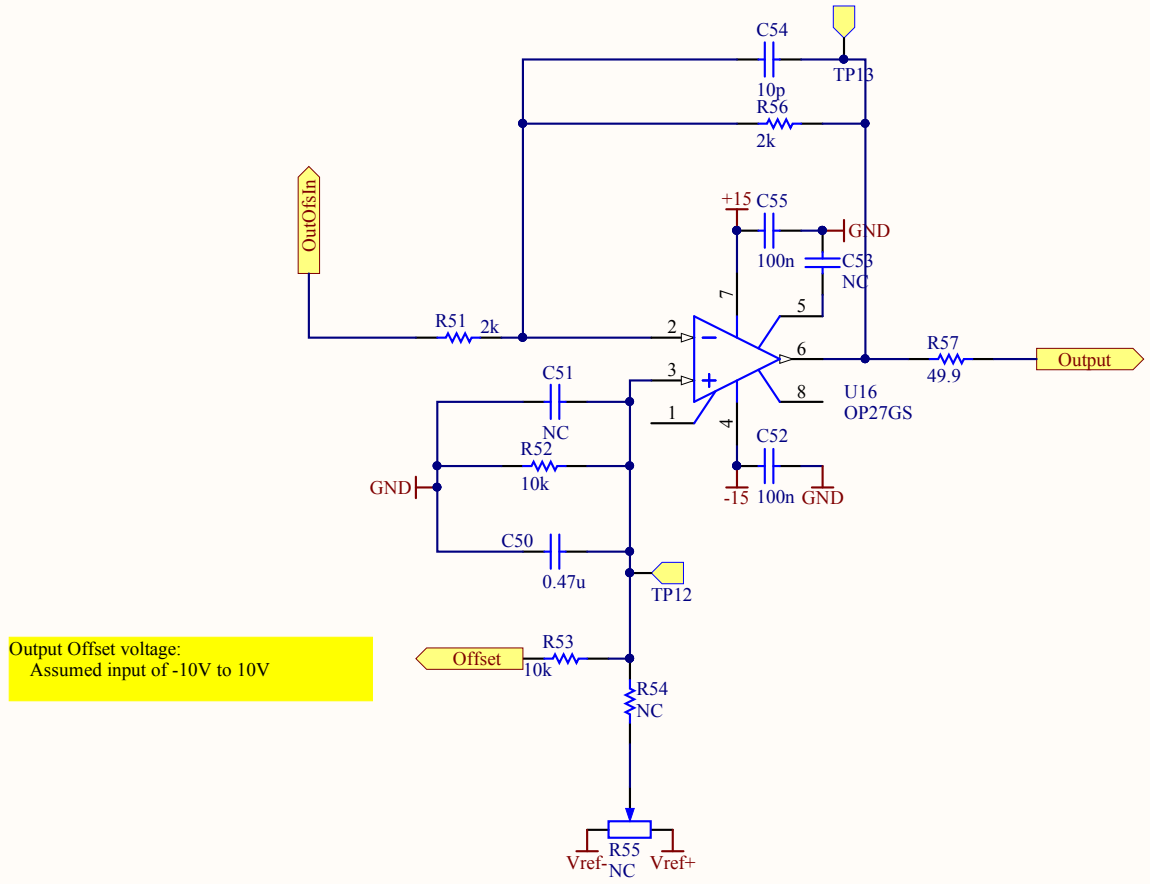
Logic = 1: Integrator
HF gain = 1
Pole at 0 Hz
Zero unchanged



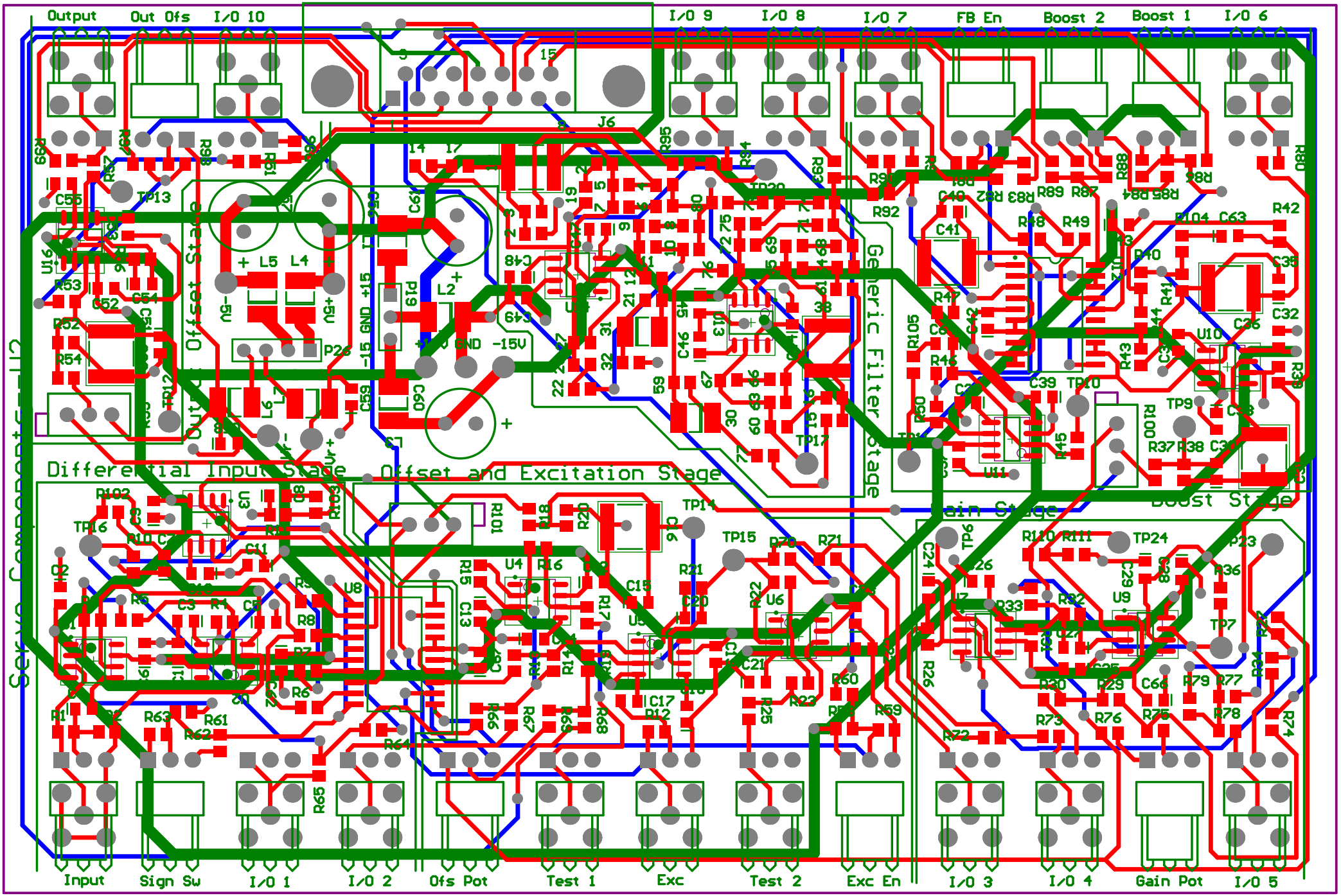

| Title | Switchable Boost/Integration stage | |
|---|---|---|
| Size: B | Number: | Revision: B |
| Date: 12/1/2014 | | Sheet of |
| File: C:\Users\..\BoostStage.SchDoc | | Drawn By: Eric Oelker |




| | | |
|---|---|---|
| Title | Generic Filter Stage | |
| Size: A | Number: | Revision: A |
| Date: 12/1/2014 | | Sheet of |
| File: C:\Users\..\GenFilterStage.SchDoc | | Drawn By: Eric Oelker |




| | | |
|---|---|---|
| Title: Output Stage | | |
| Size: A | Number: | Revision: |
| Date: 12/1/2014 | | Sheet of |
| File: C:\Users\..\OutOfsStage.SchDoc | | Drawn By: Eric Oelker |


Output
Out Ofs
I/O 10
I/O 9
I/O 8
I/O 7
FB En
Boost 2
Boost 1
I/O 6
Differential Input Stage
Offset and Excitation Stage
Generic Filter Stage
Gain Stage
Boost Stage
Input
Sign Sw
I/O 1
I/O 2
Ofs Pot
Test 1
Exc
Test 2
Exc En
I/O 3
I/O 4
Gain Pot
I/O 5